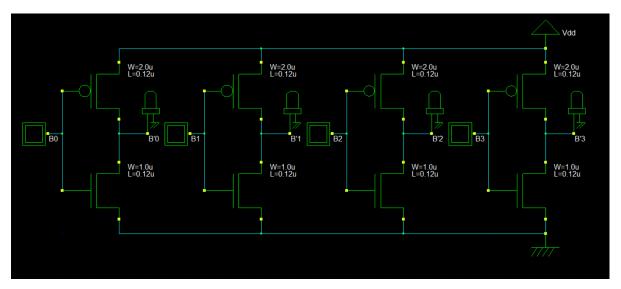
# **CMOS VLSI Design**

# Design and Simulation of a 4-bit ALU

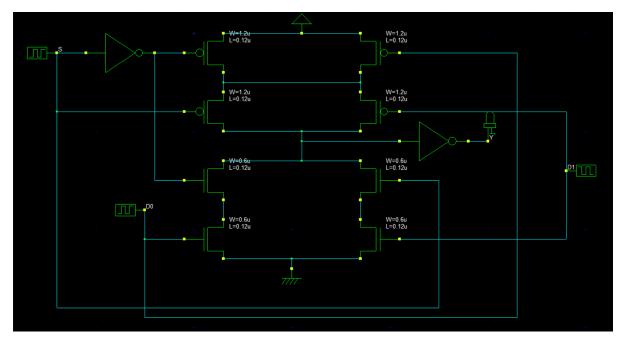
Individual components such as 4-bit inverter, 2-1 MUX, 4-bit Adder, 4-bit AND gate, 4-bit OR gate and 4-1 MUX were designed. Further, these components were connected to obtain the 4-bit ALU circuit.

## Schematics:

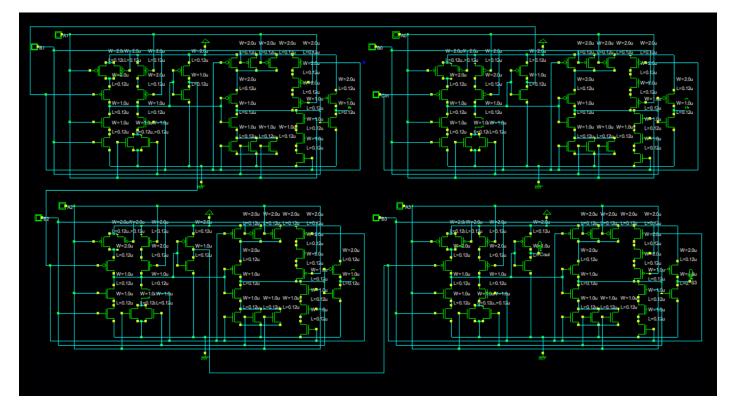
4-bit Inverter:



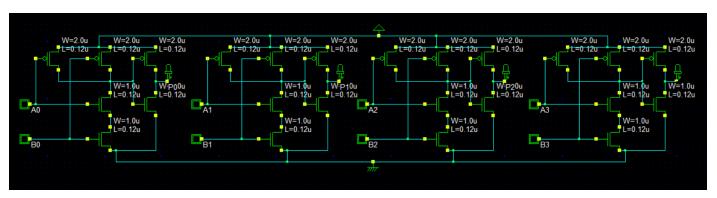
# 2-1 MUX:



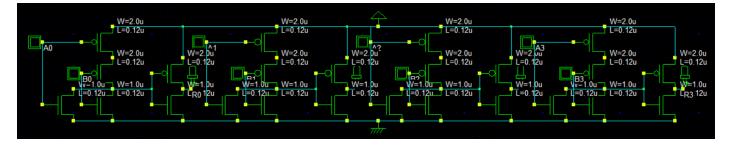
## 4-bit Adder (RCA style):



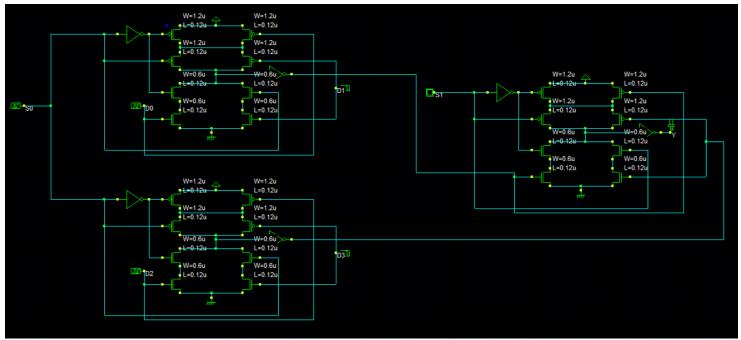
### 4-bit AND:



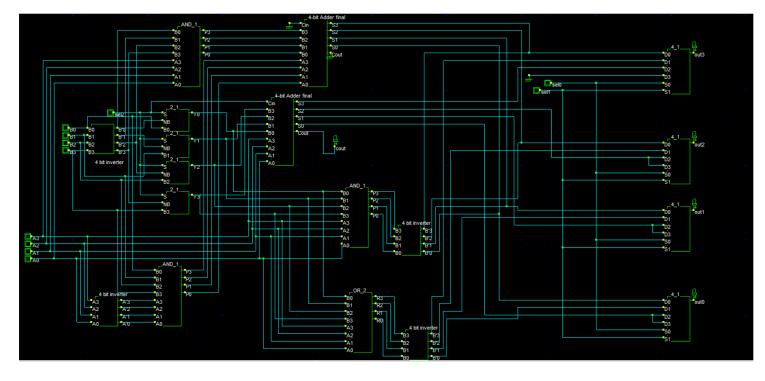
## 4-bit OR:



#### 4-1 MUX:



#### 4-bit ALU:



## Layout:

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## **Boolean Equations and Truth Table:**

Addition(4-bit): Y = A + B

Subtraction (4-bit): Y = A - B

NAND (bitwise): Y = (A&B)'

NOR (bitwise): Y = (A | B)'

XOR(bitwise): Y = A'B + AB'

Comparison (SLT) (bitwise): Y = ~ A&B

Control Signal	Operation	Output
000	NAND	(A&B)'
001	NOR	(A B)'
010	ADDITION	A+B
011	XOR	A'B + AB'
110	SUBTRACTION	A-B
111	SLT (Comparison)	(0,1) Flags

## Simulations:

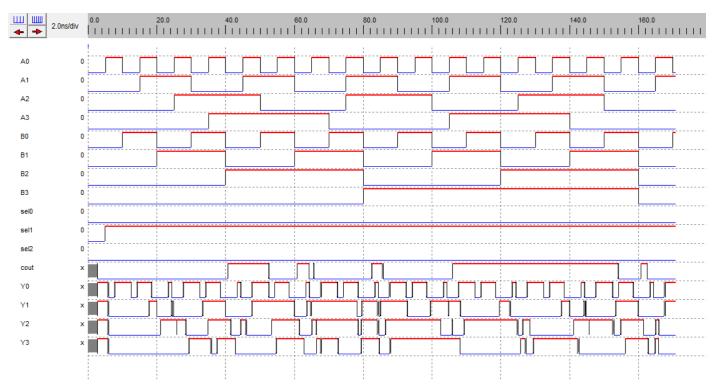
#### NAND:

Chrono View All							
2.0ns/div	0.0 20.0	40.0	60.0	80.0	100.0 12	0.0 140.0	160.0 1
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A3							
B0							
B1 B2							
B3							
sel0							
sel1							
sel2							
cout							
Y0							
Y1							
Y2							
Y3							
						i	

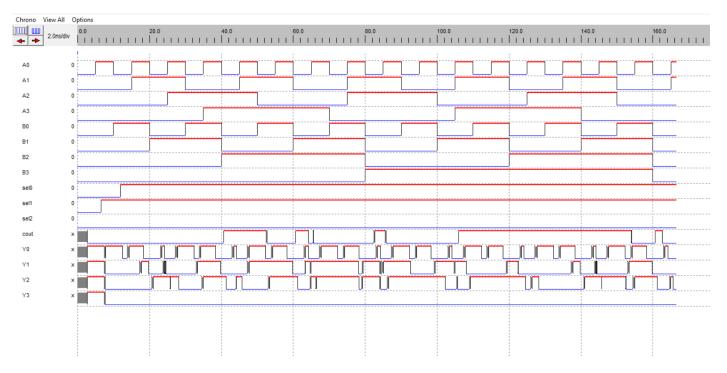
## NOR:

Ш	2.0ns/div	0.0				2	0.0				4	0.0				6	0.0				8	0.0				1(	0.00				1: 	20.0				14	0.0				10	60.0	 	
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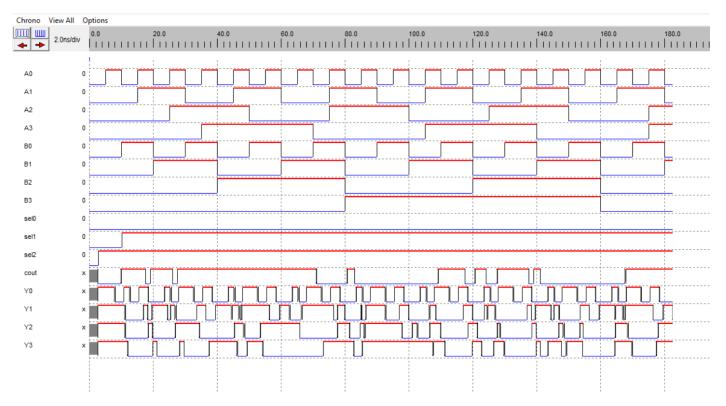
### ADDITION:



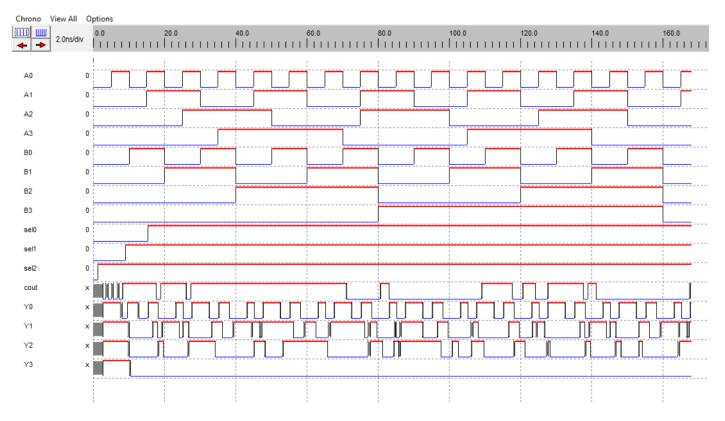
#### XOR:



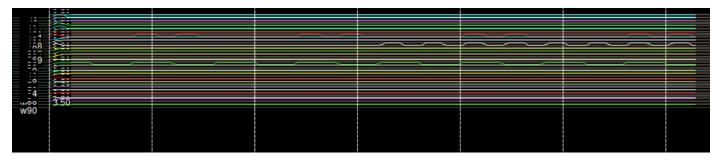
### SUBTRACTION:



# Comparison (SLT):



## Layout simulation:



#### **Reference:**

- 1. EGEC180\_Ch5.pptx (Project reference)
- 2. https://www.geeksforgeeks.org/4-bit-binary-adder-subtractor
- 3. Class notes and Presentation
- 4. https://ieeexplore.ieee.org/document/8316623